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Grant Officer:	Ms. Patsy R. Justice NASA Grants Office M.S. 500-309 NASA-Lewis Research Center 21000 Brookpark Road Cleveland, Ohio 44135
Technical Officer:	Dr. Vernon Heinen RF Technology Branch NASA-Lewis Research Center 21000 Brookpark Road Cleveland, Ohio 44135
Co-Principal Investigators:	Prof. Mark A. Smith, Prof. Vik J. Kapoor Dept. of Electrical Engineering & Computer Science University of Toledo Toledo, Ohio 43606-3390 Telephone Number: (419) 530-8000
Authorized Organizational Representative	Dr. Wayne P. Hoss Associate Vice President for Research University of Toledo Toledo, Ohio 43606 Telephone Number: (419) 530-4749

Mark A. Smith, Co-Prin. Investigator Date
Dept. Electrical Engineering and
Computer Science

Vik J. Kapoor, Co-Prin. Investigator 5-6-97 Date
Dept. Electrical Engineering and
Computer Science

FINAL REPORT

Investigation of Field Emitter Array Vacuum Microtriodes for Space Electronics Applications.

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Mark A. Smith and Vik J. Kapoor
Dept. of Electrical Engineering & Computer Science
The University of Toledo
Toledo, OH 43606-3390

ABSTRACT

Research into processing techniques for fabrication of vacuum microelectronic devices has been carried out, with special emphasis being given to the growth of silicon dioxide thin films. Oxide films ranging from 30 nm to ~2 μm have been grown on single crystal silicon wafers. Metal-oxide-semiconductor capacitor test structures have been made from some of these oxide films, and current-versus-voltage plots for these structures have been measured. It has been observed that rate of applied voltage across the oxide films produces marked differences in measured leakage current. Breakdown fields across two of the thinnest oxide films have been measured and are comparable with highest values reported in literature. Several silicon wafers were processed to make field-emitter array diodes, and were delivered to collaborators at NASA-Lewis Research Center for final fabrication steps and testing. No discoveries were made during this research effort; no patent applications were filed and none are anticipated to arise.

INTRODUCTION

The main objective of this research project was to study processing techniques used in the fabrication of vacuum microelectronic devices (VMDs). These devices consist of structures built on silicon wafers using techniques used in the manufacture of integrated circuits, but with the added feature of incorporating vacuum as the medium for electron conduction. The VMD which was fabricated and characterized for this work is based on the Spindt-type [1] diode, in which a conical cathode sits on a conductive substrate, inside a well-like cavity surrounded by an insulating thin film; on top of the insulating film is a metal thin film, with a hole in it above the conical tip, which serves as a gate for controlling electron field emission from the cathode to a collector located above the vacuum gap over the cathode. A schematic of the diode is shown in Figure 1.

The VMD of interest consists of 100 emitter cones mounted on a high-conductivity silicon wafer, on a square grid of 135 μm on each side. The emitter cones and gate layer consists of molybdenum; the cone base diameter, cone height, and gate hole diameter are each approximately 2 μm, and the gate film thickness was 0.5 μm. The insulating layer is composed of silicon dioxide grown from the substrate and is approximately 1.5 μm thick. The emitters are arranged on a square grid with a nearest-neighbor distance of 15 μm.

One of the shortcomings of the VMDs made and tested to date has been an unacceptably high gate leakage currents [2-4]. The origins of these excessive leakage currents have been attributed to poor-quality oxide films (pinholes, high concentration of defects and impurities, etc.) and poorly controlled etching of emitter wells in the oxide between the gate and substrate. In evidence of poor oxide quality have been numerous measurements on both thermally grown films and chemical vapor deposited (CVD) films which have shown breakdown field strengths significantly below ($<10^5$ V/cm) expected and desired values, i.e., $>10^6$ V/cm, which have been reported for oxides [5,6].

In an effort to improve oxide quality and to reduce gate leakage currents research activity for this grant was channeled into two thrust areas: 1) fabrication of VMDs to test concepts in processing and 2) growth of thermal oxides on silicon. Work devoted to this research was done in two phases, the first phase lasting approximately nine months and second phase lasting approximately nine months; including the six-month extension allowed for the project, the total grant period lasted for eighteen months.

In the first phase of the project, work consisted of two types of activities: 1) Travel to NASA-Lewis by one of the Principal Investigators (MAS) to learn the procedures and choice of materials which had been developed there to make some of the first VMDs evaluated during an earlier study, and 2) Installation of several key pieces of wafer processing equipment in the newly established Microelectronics Laboratory of the University of Toledo (UT). These pieces of Class 100 equipment included a wet processing station, a photoresist spin coater and a mask aligner; they joined equipment already present in the Microelectronics Laboratory for doing ellipsometry, metal thin-film deposition, CVD oxide thin-film deposition, surface analysis, sputter deposition, and rapid thermal annealing. Trips to NASA-Lewis to become acquainted with the VMD

technology took place over several months, followed by implementation of processing procedures at the Microelectronics Laboratory. During this phase, a photolithographic mask was made for the VMDs which was compatible with the UT mask aligner.

FABRICATION OF EMITTER ARRAYS

Since growth of thermal oxides on silicon could not be performed at the University of Toledo until late in the funding period, it was decided that oxide films should be grown in the furnaces of the Department of Electrical and Computer Engineering and Computer Science (ECECS) at the University of Cincinnati (UC). To that end a technical consultant, Dr. Guru Subramanyam, of Northern Iowa University, was employed during the summer of 1996 to assist in the processing of the field emitter arrays. Some of the processing steps following oxide growth were also done there to take advantage of the Reactive Ion Etching (RIE) unit available in the ECECS department. The consultant's familiarity with the equipment and personnel at the UC facility was of great benefit in expediting the processing of the arrays.

Three sets of silicon wafers were processed by the consultant. The first set of samples consisted of two (111) p-type, two (100) p-type, and 1/4 of (100) n-type wafers; the wafers were two inches in diameter. The set was cleaned at UC, and then oxidized in the ECECS department's oxidation furnace. Initial dry oxidation for two hours at 1070°C, followed by wet oxidation for 7.75 hours at 1070°C yielded a final oxide thickness close to 1.5 μm. A solution of de-ionized (DI) water with HCl in the ratio of 100:1 was used in the bubbler to minimize mobile ion contamination. The bubbler was heated to 95-98°C for two hours before oxidation was started. Subsequent testing of these samples showed excessive leakage currents, and no further processing of these wafers was done.

The second set of samples included two (100) p-type and two (100) n-type Si wafers. This set went through two cleaning procedures prior to oxidation; once again oxide thicknesses of 1.5 μm were grown at UC with a combination of dry and wet O_2 atmospheres. These samples were taken to NASA-Lewis for molybdenum deposition onto the oxide films. Molybdenum films 0.5 μm thick were deposited, without benefit of a titanium bonding layer to promote adhesion to the SiO_2. During processing of the photoresist used to expose the array hole pattern, the Mo films peeled off the wafers while in contact with developer solution. Since these samples were ruined by the Mo film lift-off, they were discarded.

A third set of wafers was then begun with some changes in processing made; this set had two each of n-type and p-type (100) Si wafers. After several cycles of cleaning, the wafers were oxidized in a UC furnace which had been used solely by a small group just for silicon thermal oxidation. A combination of dry and wet oxidation was again used, as follows: dry oxidation for 30 minutes at 1100°C, followed by wet oxidation for 5.5 hours at 1100°C. The oxygen flow rate was 0.3 liters/minute; the bubbler solution was 5 ml of HCl per 2 liters of DI water. Ellipsometry indicated a refractive index of

1.46 and an oxide thickness of 1.52 μm. Oxide on the back side of the wafers was removed by covering the top (polished) surfaces with S1813 (Shipley) photoresist, hardbaking the photoresist, and then etching the backsides with buffered HF solution.

The samples were taken to NASA-Lewis for molybdenum deposition to a thickness of 0.5 μm, this time after a deposition of 30 nm of titanium on the SiO2. Aluminum was then deposited to a thickness of 400 nm on the Mo to act as a protective layer during RIE of the emitter holes in the Mo film. Photolithography to pattern the emitter arrays was performed at NASA-Lewis and UC. Afterward, aluminum in the emitter hole regions was etched with a mixture of phosphoric, nitric and acetic acids at about 40°C. This etch produced nonuniform results across individual wafers, resulting in emitter holes typically between 2 and 4 μm in diameter. Possible improvements in processing could include elimination of the Al layer or use of a chlorine-based RIE etch of the Al.

After the photoresist was stripped, holes were RIE etched in the Mo layer with a mixture of SF_6 and O_2 (1:1) at a flow of ~10 sccm. The RIE was performed at an rf power of 200 W and a chamber pressure of 200 mT. The etch rate was ~ 150 nm/min through the Mo. After the Mo etching, silicon dioxide was RIE etched in the emitter holes using a 1:1 mixture of CHF_3 and O_2, at a flow rate of ~10 sccm, an rf power of 200 W, and a pressure of 125 mT. The etch rate for the SiO_2 was ~30 nm/min. The RIE etching of both Mo and SiO_2 were anisotropic and controlled enough not to introduce any enlargement of the emitter holes. The set of wafers was passed on to Dr. Heinen's group at NASA-Lewis for final processing by electron-beam deposition of Mo cones into the emitter holes.

THERMAL OXIDATION OF SILICON STUDIES

To study the parameters affecting growth of silicon dioxide films with desirable electrical characteristics in mind a thermal oxidation system was assembled and tested. A three-zone furnace capable of attaining temperatures up to 1200°C was purchased from Thermcraft, Inc. A quartz furnace tube and a white elephant were obtained from Quartz Scientific, Inc., as well as a quartz tray for holding wafers and quartz rods for pushing/pulling the tray in/out of the furnace tube and the white elephant. New glassware and acid-resistant plastic tubing were purchased from Fisher Scientific, along with a mantle heater, to make a bubbler unit for wet oxidation. All of the quartzware, glassware and tubing were cleaned with a dilute hydrochloric acid solution, in de-ionized (DI) water, and rinsed several times with DI water. A cylinder of ultrahigh-purity oxygen (99.999%) was hooked up to the bubbler unit through a flow controller with some additional valving so that oxidation can be done with either wet or dry O_2 under controlled flow rates.

After assembly and testing of the oxidation furnace system, more than a dozen oxide films were grown, with thicknesses ranging from 30 nm to ~2 μm. Both wet and dry oxidation runs were made, at temperatures ranging from 900 to 1100°C. More testing

and calibration of the system remains to be done. To determine breakdown fields of the oxide grown in the system, fabrication of metal-oxide-semiconductor (MOS) capacitors was done on several of the films. These capacitors were used for measuring of current-versus-voltage (I-V) curves.

Several sets of MOS capacitors were made by depositing metal thin-film dots on top of the oxide layers. The dots were approximately 5 mm in diameter, 60-200 nm thick, and composed of a gold-10% zinc alloy. The oxide films were grown on p-type (100) orientation silicon wafers (boron-doped) with resistivities in the range of 6-9 ohm-cm. The back side of the wafers were stripped of oxide with buffered oxide etch, cleaned, dried and then coated with several hundred nanometers of Au-Zn alloy. The MOS dot structures were tested in a Micromanipulator Model 6000 Test Station for I-V characteristics; applied stepped ramp voltages and measured leakage currents were achieved with a Hewlett-Packard 4140B pA Meter/DC Voltage Source. In its current configuration, the 4140B can apply up to 100 volts and can measure currents down to the picoampere range.

Early I-V plots made on oxide films 300 and 510 Angstroms thick produced an interesting time-dependent effect: the measured leakage current depended on the rate of the applied voltage across the oxide films. I-V plots obtained with 'fast' voltage ramps displayed abrupt transitions in current level, giving the appearance of 'breakdown.' I-V plots obtained with 'slow' ramps displayed slowly varying exponential-like curves in which high leakage currents were reached at voltages appreciably lower than the 'fast' ramp breakdown voltages. In Figures 2 and 3 are shown the I-V curves for oxides 30 nm and 51 nm thick, respectively. Curves are presented in each figure for a 'slow' ramp, 10 V/hr, and a 'fast' ramp, 2.5 V/s. Measureable leakage currents less than 1 mA were obtained at lower voltages for the slow ramps. It is clear that pathways of conduction through the oxide are formed regardless of ramp speed. The I-V curves for the fast ramps, however, have a more dramatic appearance, showing a sudden onset of breakdown.

Estimates of breakdown field values for the oxides calculated from the fast-ramp plots yielded field strengths of 1-2 x 10^7 V/cm. These values agreed well with published breakdown fields for SiO_2 [5,6] grown on 2 ohm-cm resistivity n-type silicon, with an applied field ramp speed of 10^6 V/cm-s. The corresponding applied field (voltage per thickness) ramp speeds shown in Figs. 2 and 3 are 8 x 10^5 and 5 x 10^5 V/cm-s, respectively. Of course, the data shown in Figs. 2 and 3 were for only two MOS dots. A more reliable measure of the oxide field strengths can only be attained after averaging over a large number of dots. Data taking for a large number of dots still remains to be done.

Another effect was observed in addition to the ramp-dependent effect. In the course of applying a voltage ramp slowly, one could stop the ramp by resetting the voltage to zero and holding it there for as long as desired, e.g. minutes or hours, noting the last highest value of leakage current. In restarting a new slow ramp from zero, one would notice that the leakage current then went immediately up to the previously obtained highest leakage current. The exact cause of the I-V response of the oxides is not known at this time. Additional work to acquire more I-V curves to probe the identifiable variables should yield an answer to the conduction problem.

CONCLUSIONS

The main objective of the funded research was to study processing techniques used in the fabrication of VMDs. This was accomplished in two ways: 1) Investigation into the thermal growth of silicon dioxide thin films on single-crystal silicon wafers and into the electrical properties of the films, and 2) Fabrication of several wafers with oxide films, deposited Mo gate layers, and etched emitter wells. Oxide films ranging in thickness from 30 nm to ~2 μm were grown on p-type (100) Si, and metal-oxide-semiconductor capacitors were made from these oxide films. Current-versus-voltage plots for some of these capacitors were measured. It was observed that the rate of applied voltage across the oxide films produced large differences in the measured leakage current. Preliminary measurements on two of the thinnest oxide films showed breakdown field strengths comparable with highest values reported in literature.

Research into improving VMD processing which remains to be done includes: 1) More extensive characterization of electrical properties of oxide films involving current-voltage and capacitance-voltage measurements; 2) Determination of conditions for reliable, reproducible film growth; 3) Characterization of oxide electrical properties as a function of silicon doping type, doping concentration, and method of oxide growth; and 4) Determination of the mechanism or mechanisms responsible for electrical conductivity. Using insights gathered from this additional work, groups involved in VMD research could then focus on processing problems attendant to emitter well etching and cone deposition and conditioning.

During the course of the research period no discoveries were made, no patent applications were filed, and no patents are anticipated to arise from the research.

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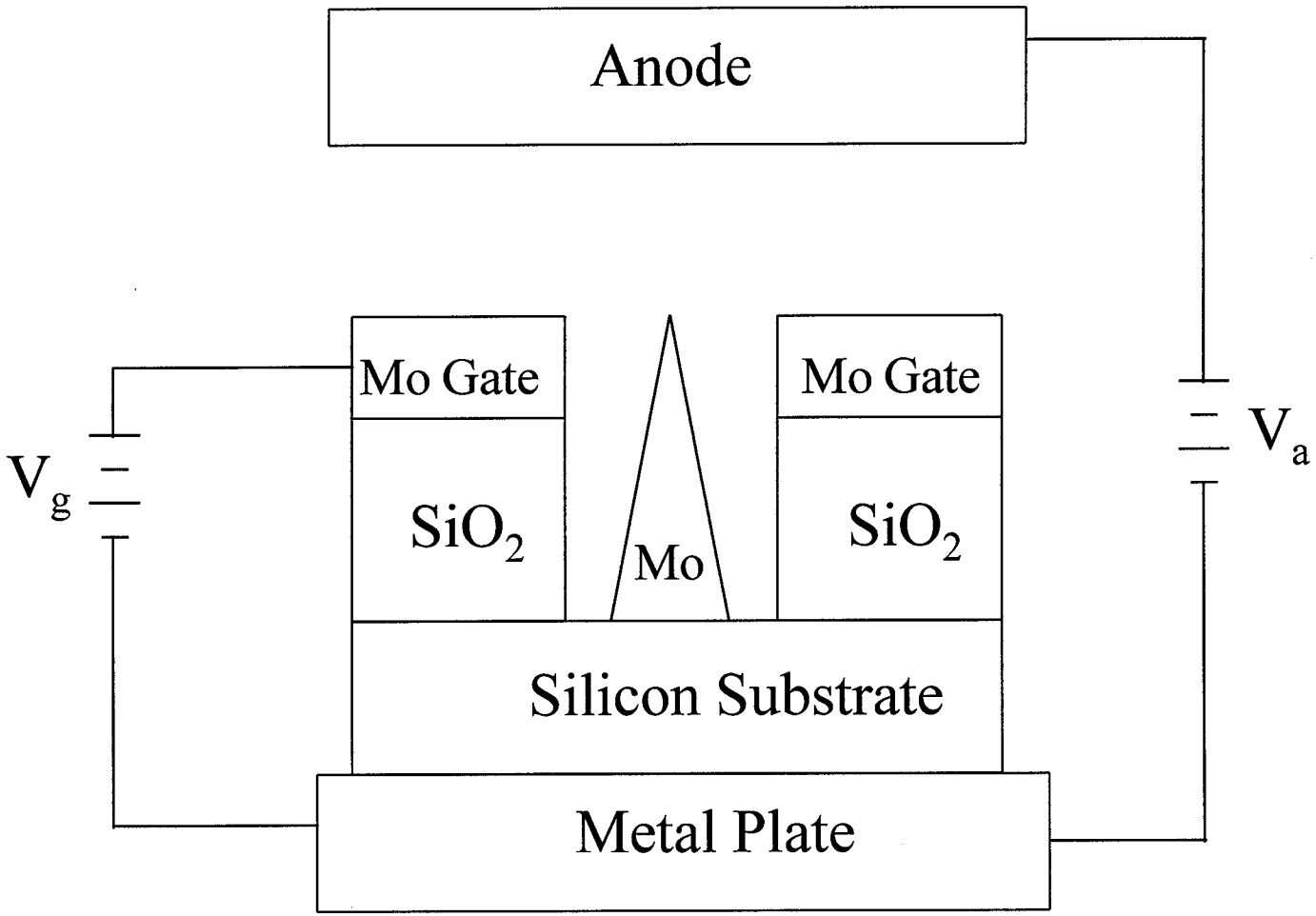
Anode
Mo Gate
Mo Gate
V_g
SiO_2
Mo
SiO_2
V_a
Silicon Substrate
Metal Plate

Figure 1

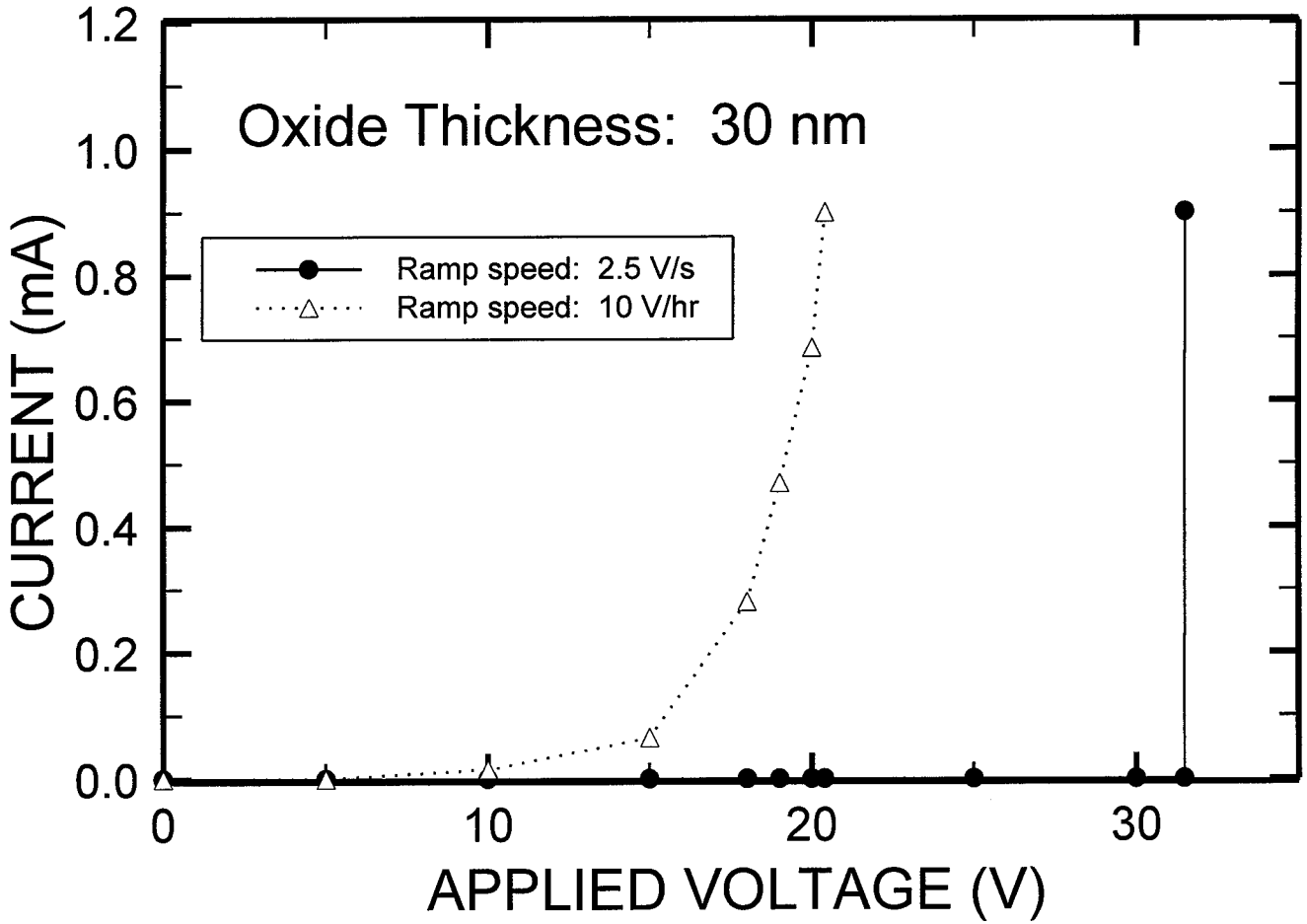
Oxide Thickness: 30 nm
Ramp speed: 2.5 V/s
Ramp speed: 10 V/hr
CURRENT (mA)
APPLIED VOLTAGE (V)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
0
10
20
30

Figure 2

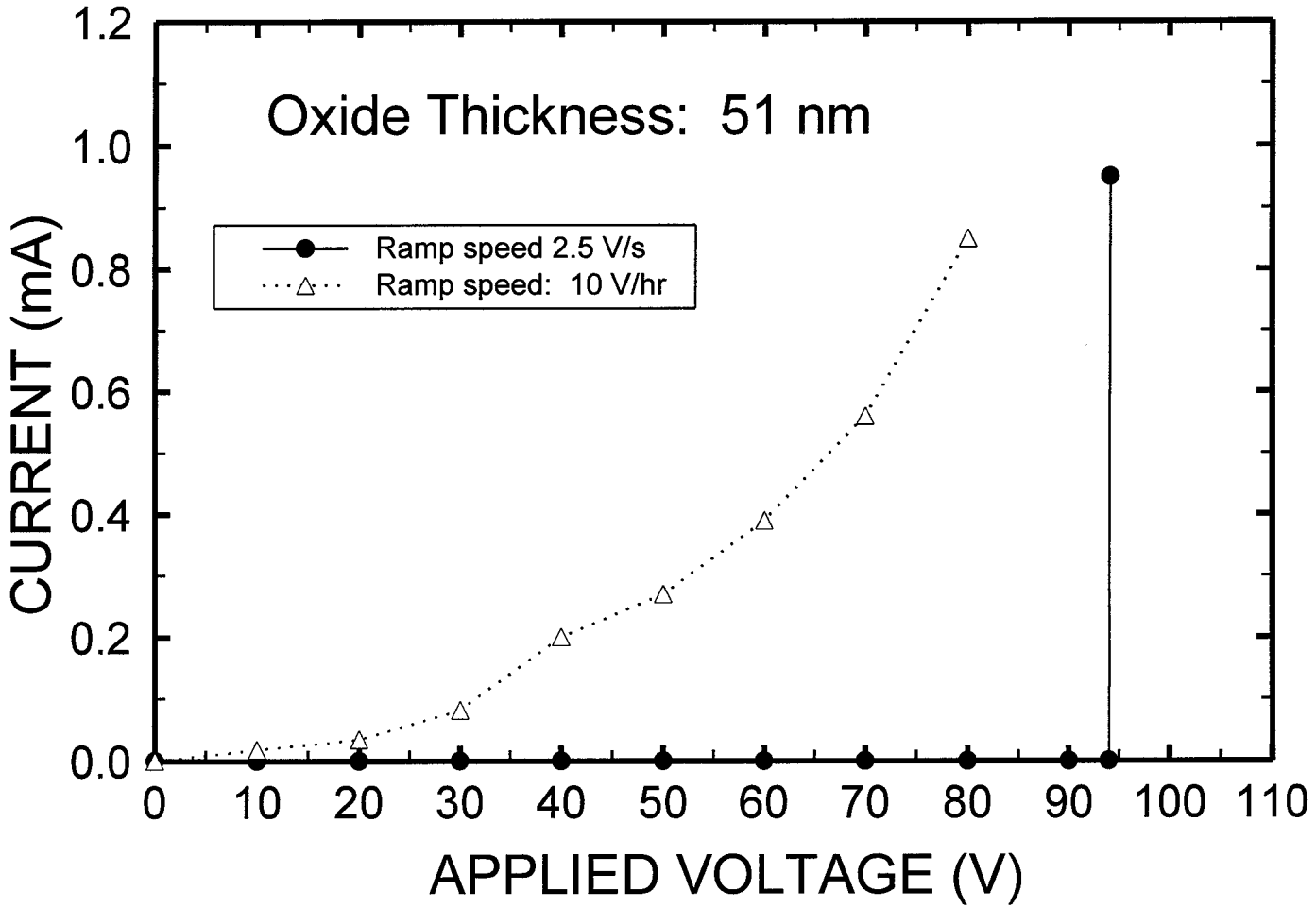
Oxide Thickness: 51 nm
Ramp speed 2.5 V/s
Ramp speed: 10 V/hr
CURRENT (mA)
APPLIED VOLTAGE (V)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
0
10
20
30
40
50
60
70
80
90
100
110

Figure 3